Claims

What is claimed is:

1. A predetermined error vector magnitude reduction circuit comprising:

an inphase register for storing digital inphase bit patterns;

a quadrature register for storing digital quadrature bit patterns;

an inphase digital-to-analog converter (DAC) for converting the digital inphase bit patterns to an inphase analog signal;

a quadrature DAC for converting the digital quadrature bit patterns to a quadrature analog signal; and

at least one lookup table containing predetermined digital inphase and quadrature bit patterns for comparison with the digital inphase and quadrature bit patterns stored in the inphase and quadrature registers, and containing modified inphase and quadrature analog data, wherein the modified inphase and quadrature analog data replaces the inphase and quadrature analog signals at the output of the DACs when there is a match between the predetermined digital inphase and quadrature bit patterns stored in the lookup table and the digital inphase and quadrature bit patterns stored in the inphase and quadrature registers.

2. The circuit of claim 1, wherein the inphase and quadrature analog signals are quantized into a plurality of levels, and wherein the modified inphase and quadrature analog signals act to modify a particular level that would otherwise result from a conversion of the inphase and quadrature bit patterns.

3. The circuit of claim 2, wherein the plurality of levels comprises 16 levels.

4. The circuit of claim 1, further comprising a storage element for storing the lookup table.

5. The circuit of claim 4, wherein the storage element is one of a group comprised of a SRAM, a DRAM, an EPROM, an EEPROM, and a Flash.

6. The circuit of claim 1, wherein the predetermined inphase and quadrature bit patterns are preloaded into at least one lookup table.

7. The circuit of claim 1, further comprising an adder for adding the inphase and quadrature analog signals.

8. The circuit of claim 7, wherein the modified inphase and quadrature analog signals are sent to the adder in place of the inphase and quadrature analog signals when there is a match between the predetermined digital inphase and quadrature signals stored in the lookup table and the digital inphase and quadrature signals stored in the inphase and quadrature registers.

9. A predetermined error vector magnitude reduction circuit comprising:

an inphase register for storing digital inphase bit patterns;

a quadrature register for storing digital quadrature bit patterns;

an inphase DAC for converting the digital inphase bit patterns to an inphase analog signal;

a quadrature DAC for converting quadrature bit patterns to an analog signal; and

at least one lookup table containing predetermined digital inphase and quadrature bit patterns for comparison with the digital inphase and quadrature bit patterns stored in the inphase and quadrature registers, and containing modified inphase and quadrature bit patterns, where the modified inphase and quadrature bit patterns replace the digital inphase and quadrature bit patterns at the input of the DACs when there is a match between the predetermined digital inphase and quadrature bit patterns stored in the lookup table and the digital inphase and quadrature bit patterns stored in the inphase and quadrature registers respectively.

10. The circuit of claim 9, further comprising a storage element for storing the lookup table.

11. The circuit of claim 10, wherein the storage element is one of a group comprised of a SRAM, a DRAM, an EPROM, an EEPROM, and a Flash.

12. The circuit of claim 9, wherein the predetermined inphase and quadrature bit patterns are preloaded into the lookup tables.

13. The circuit of claim 9, wherein the lookup table is implemented in software.

14. A transmitter comprising:

a baseband processor for generating inphase and quadrature digital bit patterns;

a predetermined error vector magnitude (EVM) reduction circuit for converting the inphase and quadrature digital bit patterns to analog signals that minimize EVM by correlating the inphase and quadrature digital bit patterns to known EVM scatter patterns;

a mixing stage for mixing the analog signal up to an RF signal;

a power amplifier for amplifying the RF signal; and

an antenna for transmitting the RF signal.

15. The transmitter of claim 14, wherein the predetermined error vector magnitude reduction circuit comprises:

an inphase register for storing the digital inphase bit patterns;

a quadrature register for storing the digital quadrature bit patterns;

an inphase DAC for converting the digital inphase bit patterns to an inphase analog signal;

a quadrature DAC for converting quadrature bit patterns to an analog signal; and

at least one lookup table containing predetermined digital inphase and quadrature bit patterns for comparison with the digital inphase and quadrature bit patterns stored in the inphase and quadrature registers, and containing modified inphase and quadrature analog signals, wherein the modified analog inphase and quadrature analog data replace the inphase and quadrature analog signals at the output of the DACs when there is a match between the predetermined digital inphase and quadrature bit patterns stored in the lookup table and the digital inphase and quadrature bit patterns stored in the inphase and quadrature registers respectively.

16. The transmitter of claim 15, wherein the inphase and quadrature analog signals are quantized into a plurality of levels, and wherein the modified inphase and quadrature analog signals act to modify the particular level that would otherwise result from the conversion of the inphase and quadrature bit patterns.

17. The transmitter of claim 14, wherein the predetermined error vector magnitude reduction circuit comprises:

an inphase register for storing the digital inphase bit patterns;

a quadrature register for storing the digital quadrature bit patterns;

an inphase DAC for converting the digital inphase bit patterns to an inphase analog signal;

a quadrature DAC for converting quadrature bit patterns to an analog signal; and

at least one lookup table containing predetermined digital inphase and quadrature bit patterns for comparing with the digital inphase and quadrature bit patterns stored in the inphase and quadrature registers, and containing modified inphase and quadrature bit patterns, wherein the modified inphase and quadrature bit patterns replace the digital inphase and quadrature bit patterns at the input to the DACs when there is a match between the predetermined digital inphase and quadrature bit patterns stored in the lookup table and the digital inphase and quadrature bit patterns stored in the inphase and quadrature registers respectively.

18. The transmitter of claim 14, wherein the mixing stage comprises a first mixer for mixing the analog signal to an intermediate frequency, followed by a second mixer wherein the intermediate frequency signal is mixed with an RF carrier to create an RF signal.

19. The transmitter of claim 14, wherein the transmitter is included in a handset that is part of a system from a group comprised of a wireless communications system, a cordless telephone system, a wireless local loop, and a satellite communications system.

20. A method for predetermined error vector magnitude reduction comprising the following steps:

testing to detect overshoot in transitions from one phase state to another at the output of a transmitter;

correlating the overshoot to particular error vector magnitude scatter patterns;

correlating the scatter patterns to particular inphase and quadrature bit patterns;

forming a lookup table containing the predetermined inphase and quadrature bit patterns and modified inphase and quadrature data for each of the bit patterns that does not cause overshoot; and

using the lookup table to prevent or reduce error vector magnitude at the output of the transmitter.

21. The method of claim 20, wherein the step of using the lookup table further comprises the steps of:

generating inphase and quadrature bit patterns;

storing the inphase and quadrature bit patterns as stored inphase and quadrature bit patterns;

comparing the stored inphase and quadrature bit patterns to the particular bit patterns; and

using the modified inphase and quadrature data when there is a match between the stored inphase and quadrature bit patterns and the particular inphase and quadrature bit patterns.

22. The method of claim 20, wherein the modified inphase and quadrature data is digital data.

23. The method of claim 20, wherein the modified inphase and quadrature data is analog data.